RECEIVER DIRECTED POWER MANAGEMENT FOR WLAN RECEIVER

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This invention is related to co-pending application of Jie Liang filed on the same date herewith entitled " METHOD AND SYSTEM FOR PROVIDING LOW POWER WLAN RECEIVER." This application is incorporated herein by reference.

FIELD OF INVENTION:

[0002] This invention relates to Wireless Local Area Network (WLAN) receiver and more particularly to reducing the power usage in WLAN receivers.

BACKGROUND OF INVENTION:

[0003] Wireless Local Area Networks (WLANs) are becoming very popular today whereby the transceiver may be small and the user no longer needs to be tied to an Ethernet cable. It is also probable that the communications device such as a wireless transceiver be a mobile battery powered device. The transceiver may be in the form of a lap top computer or a cell phone.

[0004] Because the transceiver is often used without connection to a power source through a power cord, the transceiver is therefore subject to battery drain that limits its use away from a power source. Extending the time period between battery charges is of key importance to continued communications. Various subsystems of a battery powered device may place heavier demands upon battery resources than others. When the battery powered device employs a wireless transceiver to transmit and receive

data, the transceiver typically consumes significant quantities of battery power which impacts battery life.

[0005] In order to increase the overall battery life of such transceivers, power management schemes have been utilized where the communications device enters a sleep mode where only the basic device functions such as system clock, timers, interrupts, etc. are operational. In this mode the device can neither transmit nor receive information and therefore can not perform any communication activities.

[0006] It is desirable to provide a power management system that does not impair the communications capability. Power consumption has become a major performance factor for the WLAN chipset. An important task of the IEEE 802.11a/g standard is the power consumption.

SUMMARY OF INVENTION:

[0007] In accordance with one embodiment of the present invention a method of conserving power in a WLAN receiver includes the steps of determining processing tasks that are operated only for a brief period in a packet and enabling said processing tasks during said brief period and disabling the processing thereafter until the next packet.

[0008] In accordance with an embodiment of the present invention a system for conserving power in a WLAN receiver includes a plurality of modules for performing processing tasks that occupy only a brief period for the receiver during each packet; a clock with multiple clock zones for the processing tasks; a state machine for determining the state of signal processing of a received packet; and the clock coupled to the modules and responsive to the state of the state machine for disabling the modules when processing is complete for each packet.

DESCRIPTION OF DRAWING:

[0009] Figure 1 is a block diagram of part of a WLAN receiver.

[0010] Figure 2 illustrates the ODFM processing duty cycle.

[0011] Figure 3 illustrates the WLAN receiver according to one embodiment of the present invention.

DESCRIPTION OF PREFERRED EMBODIMENT:

[0012] Figure 1 illustrates a typical WLAN network includes a transmitter TX transmitting signals over a wireless channel to a receiver RX. The transmitter TX sends the information in bursts or packets.

[0013] A typical receiver Rx receives RF signal through a diversity antenna system 21and processes the RF signal through an RF stage 23 including radio control setting 25, automatic gain control (AGC) 27 and signal diversity selection takes place. The gain control and diversity control are made at the beginning. The receiver usually has two antennas 21a and 21b and the one with the strongest signal or signal to noise ratio is selected.

[0014] The output from the RF stage is down converted using a free running local oscillator. The receiver local oscillator is free running and therefore there is usually an offset frequency from that of the transmitter local oscillator. Here is where a timing estimation and correction is done. The output from the down converter is sampled and converted to digital at an analog to digital converter (A/D) 29 and passes to a Fast Fourier

Transform module (FFT) 31 via time domain processing 30. The output from the FFT 31 is processed for channel compensation due to wireless channel fading, timing errors, and frequency offset at frequency domain processing 33. The FFT samples are also used as input to channel estimation and pilot processing module 35. The output from the channel compensator and pilot processing module 35 is applied to frequency domain processing 33 and time domain processing 30. The output from the frequency domain processing 33 is demodulated through demodulation stage 37 and then is decoded at decoding 39, descrambled at descrambler 41and applied to the MAC interface to the user.

[0015] Each packet starts with 8 microseconds of short preambles followed by an 8 microsecond long preamble followed with data symbols such as symbols 1, 2, 3 etc. Figure 2 illustrates the Orthogonal Frequency Division Multiplexing (OFDM) processing duty cycle. The first eight microseconds (t1-t8) includes the identifier at times t1-t10 during which signal detection, radio control setting, automatic gain control (AGC) and signal diversity selection takes place. During times t8 through t10 coarse frequency estimations are done for timing synchronization. The boundary of the packet is selected. There is a circuit that does a correlation to determine the type of packet as compared to other signals. It determines that it is the start of a standard 802.11 type packet as compared to other signals. At times T1 and T2 channel and fine frequency offset estimation is done.

[0016] The channel estimation is a long sequence estimation of 4 microseconds. The data symbols follow the preamble. The channel is subject to distortions such as from multi-path echo signals. The preamble contains data signals for channel estimation that are sent over the channel to the receiver RX. These data signals are known at the receiver

RX. The receiver RX compares the pattern of the received data signals from the channel to the known data signals and determines an estimate of the channel distortions (Hg). The receiver then has an equalizer at the receiver front end that applies an inverted value of the detected channel distortion (1/Hg) to substantially equalize or remove the distortions based on the channel estimate.

[0017] Also, because the channel may change during the packet a second type of equalization used is that of pilot processing where in the data symbols to follow the preamble pilot tones are inserted in each symbol for comparing to known tones to measure the error. The system then tracks the channel changes by tracking this pilot to get an offset estimation.

[0018] In accordance with the present invention the AGC module 27, boundary and packet detection module 53, the short sequence processing module 54, the channel estimation module and the radio control 25 module of receiver 51are disabled by clock signal generator or decode state machine 55 based on the state of the receiver state machine 57. See Figure 3. Figure 3 uses the same callouts for the same elements found in Figure 1. The elements that are now controlled in Figure 3 are modified to be controllable. When these detection and correction are finished the power to these modules can be saved through clock gating or gating the input data signals by the decode state machine 55.

[0019] To accomplish this more clock zones may be added to the previous clock tree and these are controlled using the receiver states as determined by the local receiver state machine. The radio control setting (RSSI/CCA portion) 25 is gated off after the preamble. The receiver automatic gain control (AGC) 27 is gated off after AGC settles.

The receiver short sequence processing 54 is gated off after short sequence processing. The receiver channel estimation/ long sequence processing 35a is shut down after long sequence processing. The boundary and packet detection 53 is gated off after that step is completed for each packet.

[0020] The channel estimation needs to be done only once for every packet and the value can be stored in a register and used for the duration of the packet. The pilot processing is active throughout the whole time following the preamble portion.

[0021] In accordance with the present invention a lot of power saving is achieved if a simpler module 35b is used exclusively for pilot processing after the preamble and a separate channel estimator 35a is operated only during the preamble of each packet. This control is provided by the decode state machine 55 identifying when the preamble is finished. The decode state machine 55 is responsive to the state of the receiver state machine and controls the power control signals to enable and disable these functions after use. A more detailed description of channel estimation and pilot processing is described in co-pending application of Jie Liang filed on the same date herewith entitled "METHOD AND SYSTEM FOR PROVIDING LOW POWER WLAN RECEIVER." This application is incorporated herein by reference.

[0022] It is estimated that by doing all of the power control described above in the receiver 51 the current power usage would change from 187 mw to 106 mw.

[0023] Although the invention has been described with reference to specific embodiments, the description is intended to be illustrative of the invention and is not intended to be limiting. Various modifications and applications may occur to those

skilled in the art without departing from the true spirit and scope of the invention as defined in the appended claims.